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09/927,058	08/09/2001	Kevin J. McGrath	5500-78200	4127

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,058	MCGRATH, KEVIN J.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/3/05* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,25-28,31-34 and 37-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _ is/are allowed.

6)☒ Claim(s) *1-7,9-15,17-22,25,26,28,31,32,34,37 and 39* is/are rejected.

7)☒ Claim(s) *8,16,27,33 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9-15, 17-22, 25, 26, 28, 31, 32, 34, 37, and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Glew et al. (U.S. Patent No. 5,721,857), herein referred to as Glew et al.'857.

Referring to claim 1, Glew et al.'857 discloses as claimed a processor (see Col. 1, line 22-23, Intel microprocessor architecture) comprising: a register (control register, see Col. 1, line 64 and Fig. 1C) configured to store a mask (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C) comprising a plurality of indications, wherein each of the plurality of indications

corresponds to (see Col. 2, lines 59-62) a respective one of a plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE inside the Status Register, see Figs. 1A and 1B); and an execution core (FPU, see col. 2, line 62) coupled to the register (control register, see Col. 1, line 64 and Fig. 1C), wherein the execution core is configured, in response to a system call instruction (see col. 3, lines 2-3, regarding operating system call (instruction) that invokes the exception handler), to selectively update a given flag of the plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) responsive to a respective indication of the plurality of indications in the mask (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C).

Referring to claim 9, Glew et al.'857 discloses as claimed an apparatus (see Col. 1, line 22-23, the system comprising Intel microprocessor architecture) comprising: a storage location (control register, see Col. 1, line 64 and Fig. 1C) configured to store a mask (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C) comprising a plurality of indications, wherein each of the plurality of indications corresponds to (see Col. 2, lines 59-62) a respective one of a plurality of flags (exception

flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B); and a processor (see Col. 1, line 22-23, Intel microprocessor architecture) coupled to the storage location (control register, see Col. 1, line 64 and Fig. 1C), wherein the processor is configured, in response to a system call instruction (see col. 3, lines 2-3, regarding operating system call (instruction) that invokes the exception handler), to selectively update a given flag of the plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) responsive to a respective indication of the plurality of indications in the mask (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C).

Referring to claim 17, Glew et al.'857 discloses as claimed a method comprising processing (by Intel microprocessor architecture, see Col. 1, line 22-23) a system call instruction (see col. 3, lines 2-3, regarding operating system call (instruction) that invokes the exception handler), the processing including selectively updating a given flag of a plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) responsive to a corresponding indication (see Col. 2, lines 59-65) in a mask (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C), wherein the mask comprises a plurality of indications and

wherein each of the plurality of indications corresponds to (see Col. 2, lines 59-65) a respective flag of the plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) and indicates whether or not the respective flag is updated in response to the system call instruction (see col. 3, lines 2-3, regarding operating system call (instruction) that invokes the exception handler).

Referring to claim 22, Glew et al.'857 discloses as claimed a processor (see Col. 1, line 22-23, Intel microprocessor architecture)comprising: a register (control register, see Col. 1, line 64 and Fig. 1C) configured to store a value (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C) that defines (see Col. 2, lines 59-65) which flags of a plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) are to be cleared in response to a system call instruction (see col. 3, lines 2-3, regarding operating system call (instruction) that invokes the exception handler) and which flags of the plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) are to be preserved in response to the system call instruction; and an execution core (FPU, see col. 2, line 62) coupled to the register (control register, see Col. 1, line 64 and Fig. 1C), wherein the execution core is configured, in response to the

system call instruction (see col. 3, lines 2-3, regarding operating system call (instruction) that invokes the exception handler), to clear one or more selected flap of a plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) and preserve one or more other flags of the plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) responsive to (see Col. 2, lines 59-65) the value (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C) in the register (control register, see Col. 1, line 64 and Fig. 1C).

Referring to claim 28, Glew et al.'857 discloses as claimed an apparatus (see Col. 1, line 22-23, the system comprising Intel microprocessor architecture) comprising: a storage location (control register, see Col. 1, line 64 and Fig. 1C) configured to store a value (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C) that defines (see Col. 2, lines 59-65) which flags of a plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) are to be cleared in response to a system call instruction (see col. 3, lines 2-3, regarding operating system call (instruction) that invokes the exception handler) and which flags of the plurality of flags are to be preserved in response to the system call instruction (see col. 3, lines 2-3, regarding

operating system call (instruction) that invokes the exception handler); and a processor (see Col. 1, line 22-23, Intel microprocessor architecture) coupled to the storage location, wherein the processor is configured, in response to the system call instruction, to clear one or more selected flags of a plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) and preserve one or more other flags of the plurality of flags responsive to the value in the storage location (control register, see Col. 1, line 64 and Fig. 1C).

Referring to claim 34, Glew et al.'857 discloses as claimed a computer accessible medium (such as the main memory of the Glew et al.'857's system) storing a plurality of instructions which, when executed in response to a system call instruction (see col. 3, lines 2-3, regarding operating system call (instruction) that invokes the exception handler), clear one or more selected flags of a plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) and preserve one or more other flags of the plurality of flags responsive to a value (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C) in a storage location (control register, see Col. 1, line 64 and Fig. 1C), wherein the value defines (see Col. 2, lines 59-65) which flags of the plurality of flags are to be cleared in response to a

system call instruction and which flags of the plurality of flags are to be preserved in response to the system call instruction (see col. 3, lines 2-3, regarding operating system call (instruction) that invokes the exception handler).

As to claims 2, 10, and 18, Glew et al.'857 also discloses: the execution core is configured to update a first flag (such as IE, see Fig. 1B) of the plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B) in response to the corresponding indication in the mask being in a first state (the state when mask bit IM =1, see Col. 2, lines 59-65) and wherein the execution core (FPU, see col. 2, line 62) is configured to retain a current state of the first flag (such as IE, see Fig. 1B) in response to the corresponding indication in the mask.

As to claims 3, 11, and 19, Glew et al.'857 also discloses: the execution core is configured to update the first flag (such as IE, see Fig. 1B for indicating the invalid operation status) by clearing the first flag (when mask bit IM is unmasked, i.e. IM =0, see Col. 2, lines 59-65).

As to claims 4, and 12, Glew et al.'857 also discloses: the corresponding indication is a bit (the mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C).

As to claims 5, and 13, Glew et al.'857 also discloses: the first state (the state when mask bit IM =1, see Col. 2,

lines 59-65) comprises the bit being set (the state when mask bit IM is set to "1", see Col. 2, lines 59-65).

As to claims 6, 14, and 20, Glew et al.'857 also discloses: the execution core is coupled to receive an indication of an operating mode of the processor, and wherein the execution core is configured to selectively update the given flag in a first operating mode (the operating mode when mask bit IM is unmasked, e.g., IM =0, see Col. 2, lines 59-65, regarding the exception handler is invoked. Therefore, the given flag is updated), and wherein the execution core is configured not to perform a selective update in a second operating mode (the operating mode when mask bit IM is masked, e.g., IM =1, see Col. 2, lines 59-65, regarding the processor takes an appropriate default action and continues with computation. Therefore, the given flag is not updated).

As to claims 25, and 31, Glew et al.'857 also discloses: the execution core is coupled to receive an indication of an operating mode (the operating mode when some mask bits IM are unmasked, e.g., IM, DM, and ZM =0, see Col. 2, lines 59-65, regarding the processor takes an appropriate default action and continues with computation. Therefore, the given flags IE, DE, and ZE will be updated) of the processor, and wherein the execution core is configured to clear one or more selected flags

and preserve one or more other flags (the other unchanged flags, such as OE, UE, and PE, see Fig. 1B in the exception flags) in a first operating mode.

As to claims 7, 15, 21, 26, and 32, Glew et al.'857 also discloses: the execution core is configured to perform a predetermined update (note initializing the values of IE, DE, ZE, OE, UE, and PE, see Fig. 1B in the Glew et al.'857's system is best reasonably and broadly interpreted as performing a predetermined update) of the plurality of flags (IE, DE, ZE, OE, UE, and PE, see Fig. 1B) in the second operating mode (the operating mode when mask bit IM is masked, e.g., IM =1, see Col. 2, lines 59-65, regarding the processor takes an appropriate default action and continues with computation. Therefore, the given flag is not updated). Note "a fixed update" in claim 21, line 1 is interpreted as "a predetermined update" as set forth in claim 7, line 2.

As to claim 37, Glew et al.'857 also discloses: the plurality of instructions, when executed in a first operating mode (the operating mode when some mask bits IM are unmasked, e.g., IM, DM, and ZM =0, see Col. 2, lines 59-65, regarding the processor takes an appropriate default action and continues with computation. Therefore, the given flags IE, DE, and ZE will be updated), clear the one or more selected flags (as set forth

above, when some mask bits IM are unmasked, e.g., IM, DM, and ZM =0, see Col. 2, lines 59-65, regarding the processor takes an appropriate default action and continues with computation. Therefore, the given flags IE, DE, and ZE will be updated by such as clearing) and preserve the one or more other flags (the other unchanged flags, such as OE, UE, and PE, see Fig. 1B in the exception flags), and wherein the plurality of instructions, when executed in a second operating mode (the operating mode when mask bit IM is masked, e.g., IM =1, see Col. 2, lines 59-65, regarding the processor takes an appropriate default action and continues with computation. Therefore, the given flag is not updated) perform a predetermined update (note initializing the values of IE, DE, ZE, OE, UE, and PE, see Fig. 1B in the Glew et al.'857's system is best reasonably and broadly interpreted as performing a predetermined update) of the plurality of flags.

As to claim 39, Glew et al.'857 also discloses: the value in the storage location (control register, see Col. 1, line 64 and Fig. 1C) comprises a mask (FPU control word comprising mask bits IM, DM, ZM, OM, UM, and PM, see col. 2, lines 60-61, and Fig. 1C) having a respective indication (see Col. 2, lines 59-62) for each of the plurality of flags (exception flags, IE, DE, ZE, OE, UE, and PE, see Fig. 1B).

Allowable Subject Matter

3. Claims 8, 16, 27, 33, and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments mailed 1/3/05 have been considered but are moot in view of the new ground(s) of rejection. As set forth in the art rejections above, Glew et al.'857 teaches the claimed invention.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this

action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC central telephone number, (571)272-2100.

7. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly **into the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

February 18, 2005